Title: TWO-WIRE INTERFACE HAVING EMBEDDED PER
FRAME RELIABILITY INFORMATION
Inventors: Gerald L. Dybsetter and Jayne C. Hahin
Docket No.: 15436.367.1

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Fig. 1

Fig. 2

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```
                                                        (TA)                              (SLAV-STUS)
         H  OP          XTND  ADDR         BH   DATA_H  DATA_L   CRC       BT2 Z3   SP
     PRE SR    DEV           Z0       BT1   Z1             Z2           ACK E
     7 6 5 5 5 5 5  4 4 4 4  3 3 3 3  2 2 2 2  1 1 1 1      0 0 0 0
     4 0 9 8 7 6 4 3 1 0 3 2 1 4 3 2 1 4 3 2 1 4 3 2 1 5 4 3 5 4 3 2 1 0

RD:  H...H 1 00 101 VVV XXXXXXX 0 AAAAAAA Z B DDDDDDD 0 DDDDDDD 0 CCCCCCC 0 1 0 0 1z --301A
moe: .  *  ** *** *** ******* . .* ******* . .* ******* .* ....* ....* .: .* --302A
soe: .  .  .: .. .. ....... . . . .* .* . .* .: .* --303A

WR:  H...H 1 00 001 VVV XXXXXXX 0 AAAAAAA 0 1 DDDDDDD 0 DDDDDDD 0 CCCCCCC z 1 0 0 1z --304A
moe: .  *  ** *** *** ******* .* ******* .* ****** .* ....* .* --305A
soe: .  .  .: .. .. ....... . .: .* .* . . .* .: .* --306A

crc_gen: .  .: *** *** ******* ..* ******* ****** *** ....* --307A
crc_chk: .  .: *** *** ******* . . .: ****** *** . .* --308A

     <----|
          |__|
     +----+
     (restart if input not all 1's)
```

Fig. 3A

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```
                                                                    (TA)                                    (SLAV-STUS)
                          H   SR   OP   DEV   ADDR   BT1 DATA_H   BH   Z1 DATA_L   Z2  CRC   Z3 SP   ACK E
                      PRE                                                                                    BT2 Z3  SP
                      6 5   4 4   4 4   4 4   4           3 3 3   3    2 2 2   2 2   1 1 1           0 0 0 0  0 0
                      5 0   9 8   7 5   4 2   1           4 3 2   1    4 3 2   2    5 4 3           6 5 4 3 2 1 0

RD: H...H  1 00 100 VVV AAAAAAAA   Z B DDDDDDDD  0 DDDDDDDD 0 CCCCCCCC 0 1 0 0 1z  ←301B
moe: *     * *  ***  ***  ********  . . .********  . *  .********  . *  .  :  . : *
soe: .     . .  .    .    .   *      .   ********  . *  .********  . *  . : * .*.

WR: H...H  1 00 000 VVV AAAAAAAA   0 1 DDDDDDDD  0 DDDDDDDD 0 CCCCCCCC Z 1 0 0 1z  ←304B
moe:       * *  ***  ***  ********  . * .********  . *  .********  . *  .  :  . : *
soe:       . .  .    .    .   *      . . .*  .     .   .********  . *  . : * .*.

                 *    *   *    *   ********  . . .*  . *  .  ********  . *  . . : *
crc_gen:  .      . .  ***  ***  ********  . . .********  . *  .********  . *  .  . : *
crc_chk:  .      . :  :    :    ********  . . .  ****   * *  .  ****   * *  . : *  .*.

        ^
        |    (restart if input not all 1's)
      +-+-+
```

Fig. 3B

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```
      H                              BH              Z1          Z2
PRE   SR   OP   DEV  ADDR     BT1 DATA_H     DATA_L        SP
      33   33   33   2        22  2 1 1 1   1 1 0 0 0    0 0
5     33   33   32   2        21  0 9 8 7   2 1 0 9 3    2 1 0
3     98   76   09   9        10                         3
---   ---  ---  ---  ---      --  ---------  ----------  -----
RD:   H..H 1 00 110  VVV  AAAAAAA  Z B DDDDDDDD  O DDDDDDDD  O 1Z   ←~301C
moe:       ***  *** *** ********   . . :******  . :******* . :*
soe:  * .  *    .   . .  ........  . * ********  . :*******  . :*

      ---  ---  ---  ---      --  ---------  ----------  -----
WR:   H..H 1 00 010  VVV  AAAAAAA  0 1 DDDDDDDD  O DDDDDDDD  O 1Z   ←~304C
moe:  *    *    *** *** ********   * ********   * ******** * :*
soe:  . .  .    .   . .  ........  * ........  . ........  . :*

<___|   |__+      (restart if input not all 1's)
    +___|
```

Fig. 3C

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Master Component

401 — Determine Operation To Be Performed

402 — Begin Transmitting Frame

404 — Transfer Control Of Data Wire

407 — Receive Remaining Portion Of Frame

Slave Component

403 — Receive A Portion Of Frame

405 — Receive Control Of Data Wire

405 — Transmit Remaining Portion Of Frame

400

Fig. 4

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Fig. 5

Laser Transmitter / Receiver 500

To Host ← 502A

Post-Amplifier 502 ← Receiver 501

From Host ← 503A

505A

Laser Driver 503 → Transmitter 504

505B

SCL
To / From Host
SDA

Control Chip 505
Analog 508

Memory 506

510A

510B

Fig. 5

Fig. 6

Digital Portion 600

Timers 602

Processor 603A

Memory Controller 607

Processor 603B

Host Communication Interface 604 | SIC 601A

Memory 606

SIC 601B | External Device Interface 605

Input / Output Multiplier 608

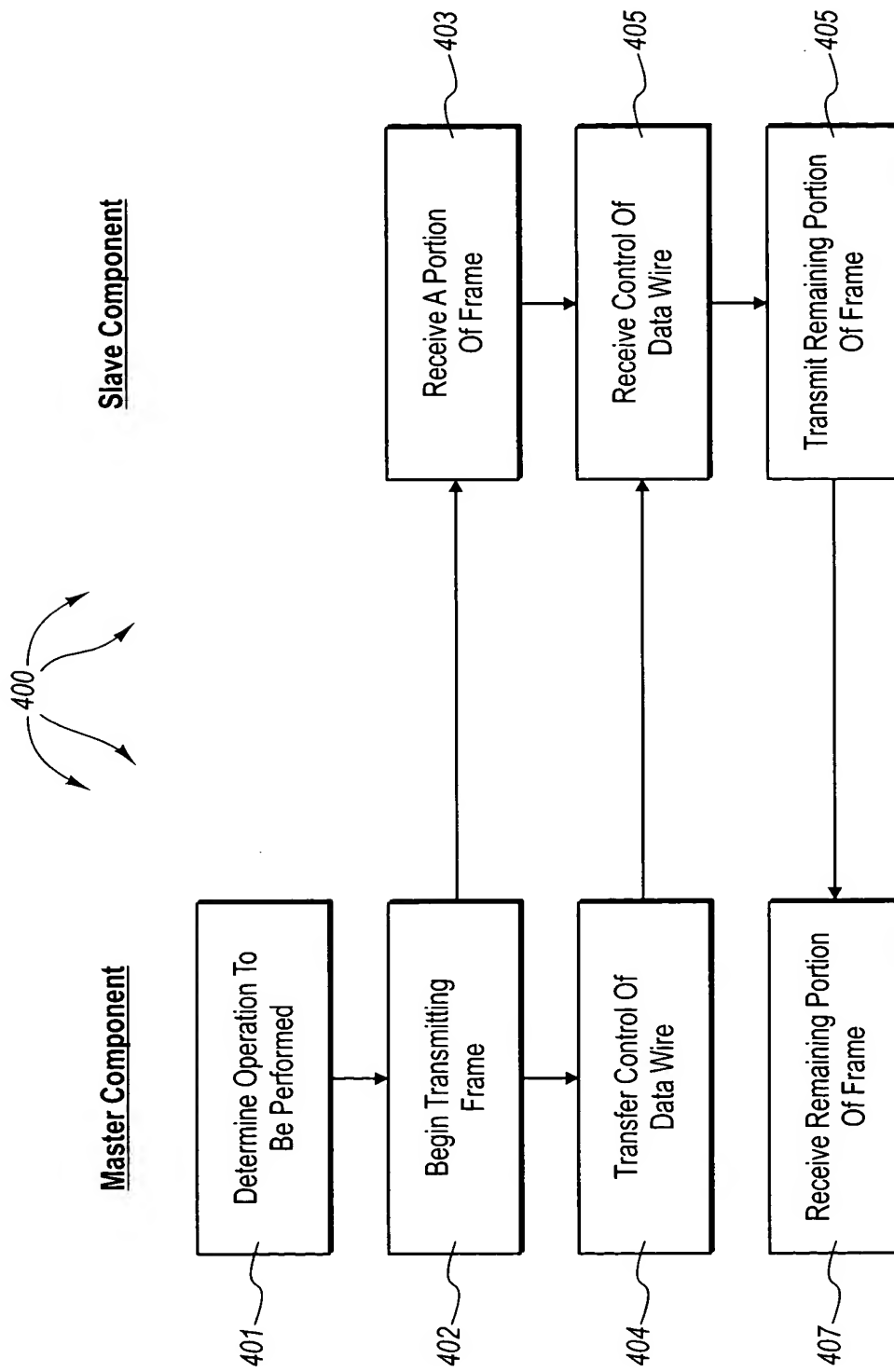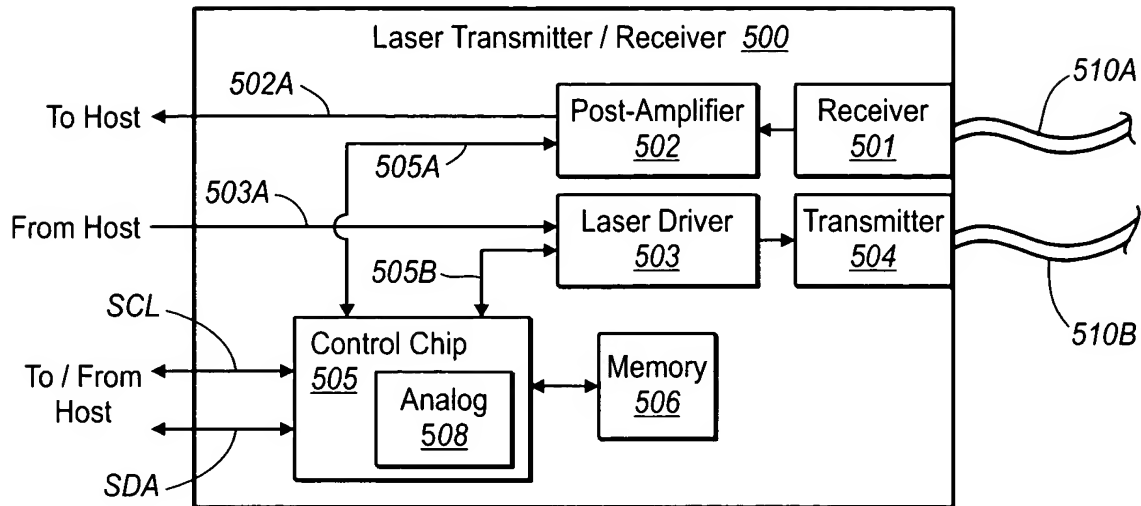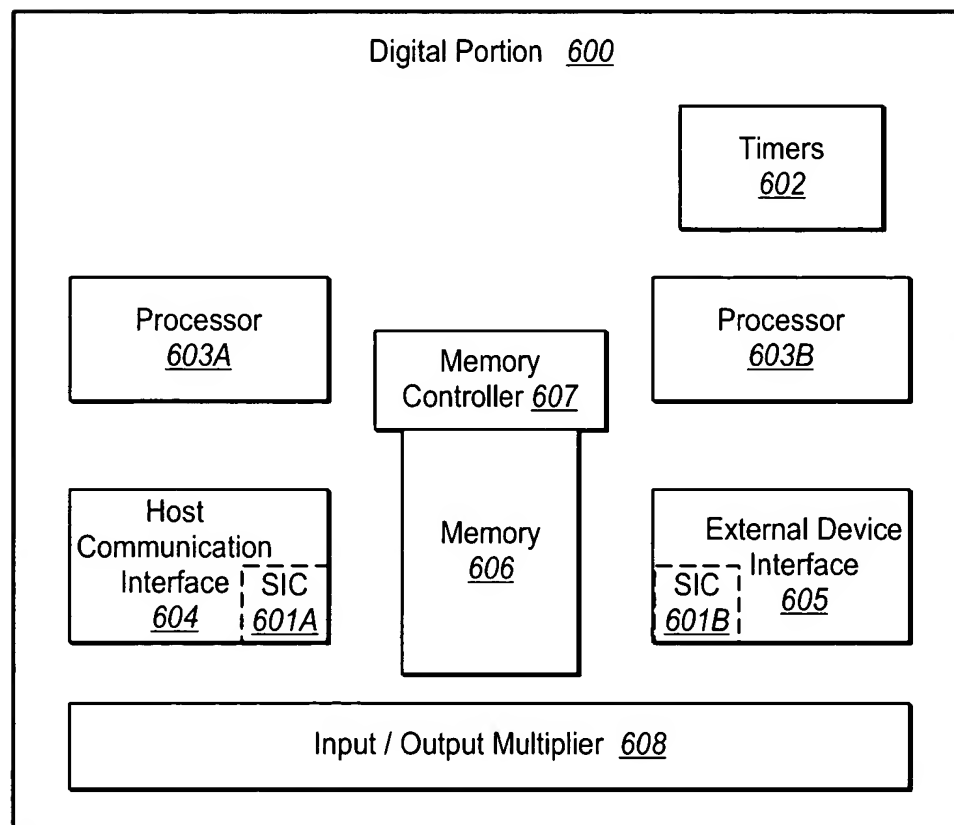**Fig. 6**

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	PRE	ST	OP	PRT	DEV	TA	ADDRESS/DATA	IDLE
	6	3 3	3 2	2	2	1 1	1	0 0
	4	3 1	0 9	8	4 3	8 7	6	1 0
Address	1...1	0 0	0 0	PPPPP	EEEEE	1 0	AAAAAAAAAAAAAAAA	Z
Write	1...1	0 0	0 1	PPPPP	EEEEE	1 0	DDDDDDDDDDDDDDDD	Z
Read	1...1	0 0	1 1	PPPPP	EEEEE	Z 0	DDDDDDDDDDDDDDDD	Z
Read inc.	1...1	0 0	1 0	PPPPP	EEEEE	Z 0	DDDDDDDDDDDDDDDD	Z

Field	Bits	
PRE	64:33	(32) -- preamble
ST	32:31	(2) -- start of frame
OP	30:29	(2) -- operation code
	(ADDR=00,WR=01,RD=11,RDINC=10)	
PRTAD	28:26	(5) -- port address
DEVAD	25:19	(5) -- device address
TA	18:17	(2) -- bus turnaround phase & transfer acknowledge
ADDR/DATA	16:1	(16) -- address or data
IDLE	0	(1) -- end of transmission
	65	-- transaction bit length

Fig. 7
(Prior Art)